## REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-7 and 9 are pending in the present application. Claims 1-3, 7 and 9 have been amended and Claims 8 and 10-25 have been canceled by the present amendment.

In the outstanding Office Action, Claims 1, 3, 4 and 6 were rejected under 35 U.S.C. § 103(a) as unpatentable over Jaso et al.; and Claim 9 was rejected under 35 U.S.C. § 103(a) in view of Jaso et al. in view of Kita.

Claims 1, 3, 4 and 6 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Jaso et al. This rejection is respectfully traversed.

Amended Claim 1 is directed to a semiconductor device including a first semiconductor layer formed above a first region of a supporting substrate with a first buried oxide layer disposed therebetween, and a second semiconductor layer formed on a second region of the supporting substrate. Further, an interface between the supporting substrate and said second semiconductor layer is placed in a position deeper than the buried oxide layer.

In a nonlimiting example, Figure 7 illustrates an interface JS between the supporting substrate 31 and the second semiconductor layer 34 being placed in a position deeper than the buried oxide layer 32.

The claimed structure has an advantage in that when a MOSFET is formed by constructing a DRAM cell transistor and a cell capacitor in the second semiconductor layer and a logic circuit in a first semiconductor region of the supporting substrate, a depletion layer and impurity diffusion layers serving as the source and drain region of the cell transistor do not cross the interface of the substrate and the second semiconductor layer. Thus, an increase in the leak current and a decrease of pause characteristics is suppressed, thereby

increasing the electric characteristics of a device formed on a non-SOI region (bulk region) on a partial SOI substrate.

On the contrary, Jaso et al. only discloses an "SOI/bulk hybrid substrate" in which the interface between the substrate 12 and the bulk device region 122 (second semiconductor layer) is placed at the same depth as the lower surface of the insulative layer 14 (buried oxide layer). Jaso et al. does not teach or suggest a structure in which the interface is placed in a position deeper than the buried oxide layer as claimed.

Accordingly, it is respectfully submitted independent Claim 1 and each of the claims depending therefrom are allowable.

Claim 9 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Jaso et al. in view of Kita. This rejection is respectfully traversed.

Claim 9 depends indirectly on Claim 1, which as discussed above is believed to be allowable. Further, Kita discloses a trench type DRAM formed across the buried oxide layer. However, Kita does not teach or suggest a structure in which the surface between a substrate and a second semiconductor layer is placed at a position deeper than a buried oxide layer. Accordingly, it is respectfully requested this rejection also be withdrawn.

Further, the specification (Brief Summary of the Invention) and the abstract have also been amended to correspond with the changes made to Claim 1.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

22850

Tel: (703) 413-3000
Fax: (703) 413-2220

I:\ATTY\DAB\219723US-AM.DOC

Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870
David A. Bilodeau
Registration No. 42,325